WHAT IS CLAIMED IS:

1. A SRAM cell comprising:

a pair of access devices;

a pair of pull-up devices;

a pair of pull-down devices; and

at least one metal plate formed on metal interconnection lines in contact with a substrate, having a dielectric film interposed between the metal plate and the metal interconnection lines, so as to increase a cell capacitance, thereby reducing a soft error rate.

2. A SRAM cell as claimed in claim 1, wherein one metal plate is included in each cell.

3. A SRAM cell as claimed in claim 2, wherein the metal plate overlaps with a first one of a metal interconnection line of a node side and a metal interconnection line of a node bar side, while being in contact with a second one of the metal interconnection line of the node side and the metal interconnection line of the node bar side.

4. A SRAM cell as claimed in claim 1, wherein two

metal plates are included in each cell.

5. A SRAM cell as claimed in claim 4, wherein the metal plates overlap, respectively, with one metal interconnection line different from each other of a metal interconnection line of a node side and a metal interconnection line of a node bar side, while being in contact with another metal interconnection line of the node side or the node bar side which are opposite to the contacted metal interconnection line, respectively.

6. A method of manufacturing an SRAM cell, the method comprising the steps of:

(1) forming a gate on a semiconductor substrate having an isolation layer;

(2) depositing an interlayer insulating film on the substrate so as to cover the gate;

(3) etching the interlayer insulating film to form contact holes which expose the gate and the substrate, respectively;

(4) filling each of the holes with a conductive film to form contact plugs;

(5) sequentially depositing an etching barrier film and an insulating oxide film on the interlayer insulating film

including the contact plugs;

(6) etching the insulating oxide film and the etching barrier film to form trenches of predetermined shapes which expose respective contact plugs;

(7) filling each of the trenches with a metal film to form metal interconnection lines;

(8) depositing a dielectric film on the insulating oxide film including the metal interconnection lines;

(9) etching the dielectric film to expose at least one specified metal interconnection line; and

(10) forming a metal plate so that the metal plate is in contact with the metal interconnection line exposed out of the dielectric film.

7. A method of manufacturing an SRAM cell as claimed in claim 6, wherein the contact plug is a tungsten plug including a barrier metal film.

8. A method of manufacturing an SRAM cell as claimed in claim 6, wherein the dielectric film comprises either an oxide film made from an oxide selected from the group consisting of PE-TEOS, HTO, and MTO or a nitride film made from a nitride such as Si_3N_4.

9. A method of manufacturing an SRAM cell as claimed in claim 6, wherein the deposited dielectric film has a thickness of 200~600 Å.

10. A method of manufacturing an SRAM cell as claimed in claim 6, wherein step (9) is performed under a condition in which surface loss of the metal interconnection line caused by over-etching is maintained less than 500 Å.

11. A method of manufacturing an SRAM cell as claimed in claim 6, wherein the metal plate is made from one material selected from the group consisting of Ti, TiN, and Ti/TiN.

12. A method of manufacturing an SRAM cell as claimed in claim 6, wherein the formed metal plate has a thickness of 100~500 Å.

13. A method of manufacturing an SRAM cell as claimed in claim 6, wherein step (9) is performed so that one of a metal interconnection line of a node side and a metal interconnection line of a node bar side is exposed.

14. A method of manufacturing an SRAM cell as claimed in claim 13, wherein one metal plate is formed in each cell,

the metal plate being in contact with an exposed metal interconnection line of the metal interconnection lines of the node side and the node bar side, the metal overlapping with another metal interconnection line of the node bar side or the node side which are opposite to the contacted metal interconnection line.

15. A method of manufacturing an SRAM cell as claimed in claim 6, wherein step (9) is performed so that both a metal interconnection line of a node side and a metal interconnection line of a node bar side are exposed.

16. A method of manufacturing an SRAM cell as claimed in claim 15, wherein two metal plates are formed in each cell, two metal plates being in contact with the exposed metal interconnection lines of the node side and the node bar side respectively, each metal plate overlapping with the metal interconnection line of the node side or the node bar side which are opposite to the contacted metal interconnection line, respectively.